Remarks:

The issues were addressed in the interview summary by discussing the examiner's Response to Arguments first.

Response to Arguments

1. The examiner states that the relationship between the LVTSCR structure and the additional p+ region and additional n+ region is not clear.
   It is respectfully pointed out that an LVTSCR has a specific and known structure that is shown not only in Figure 2 and the Background discussion of the present application, but is also shown in Figure 3 of Ker.
   Furthermore, the structural features of an LVTSCR are explicitly recited in the claims to avoid any ambiguity.
   The additional p+ and n+ regions in the p-well are then explicitly recited as being in addition to the already existing p+ and n+ region of a standard LVTSCR.
   There is therefore no ambiguity about the fact that claim 2 requires at least two p+ and at least two n+ regions in the p-well (one p+ region and one n+ region as found in a standard LVTSCR and at least one additional p+ region and at least one additional n+ region in accordance with the invention).
   This feature is missing from Ker and distinguishes the present claims from Ker.

2. The examiner states that it is unclear how a junction, which is the boundary between two elements can comprise more than two elements.
   Claim 2 has been amended to clarify that each junction between a p-type material and an n-type material forms one diode. However, claim 2 states that at least one additional p+ region and at least one additional n+ region is formed in the p-well. Therefore some embodiments may have more than one additional p+ and more than one additional n+ region in the p-well and can therefore form more than one p-n junction. This is, for instance, illustrated in Figure 4 of the application.

3. The examiner states that the method of increasing holding voltage of an LVTSCR is inherent in Ker.

   Ker states that its purpose is to decrease the triggering voltage, not increase the holding voltage (see col. 1, lines 15-59). It uses a prior art approach to address holding voltage issues. In particular it uses a silicon over insulator (SOI) process to address holding voltage problems as discussed at column 1, lines 21-24. In addition it shows an embodiment in Figure 10 A that has external diodes.

   The use of external diodes is discussed as one prior art solution in the Background section to the present application, where the problems of this approach are laid out. In particular, as stated in the last paragraph of the Background to the Invention: "*One proposed solution to increasing the holding voltage of a LVTSCR has been to provide a circuit in conjunction with the LVTSCR which increases the holding voltage by introducing a voltage drop in the form of one or more diodes. This is illustrated in Figure 3 in which a diode 300 is connected in series with the LVTSCR 302 between V_{dd} and ground. The problem with such an isolated diode or diodes string is that it increases the parasitic capacitance and consumes more space. Furthermore, it is not suitable for all CMOS processes and therefore does not lend itself steadily to implementation using existing process technology.*"

   Thus the only thing inherent in Ker is the prior art approach of a SOI process to increase holding voltage and using external diodes. As discussed above, Ker does not include the additional p+ and n+ regions in the p-well for forming the internal diode structures of the invention.

35 USC 112

Claim 2 was rejected as unclear as to which elements are the additional p+ regions and the additional n+ regions.

As discussed above, an LVTSCR has a specific and known structure that is shown not only in Figure 2 and the Background discussion of the present application, but is also shown in Figure 3 of Ker. In Figure 4 of the present application, the first n+ region and

first p+ region in the n-well 400 is given by 406 and 408. The second n+ region and second n+ region in the p-well 402 is given by 412 and 420. A gate 414 is located between the high voltage node (anode) defined by the first n+ region and first p+ region, and the low voltage node (cathode) defined by the second n+ region and second p+ region These structural features of an LVTSCR are explicitly recited in the claims to avoid any ambiguity.

Claim 2 has been amended to only require only one additional n+ region in the p-well. This additional n+ region is given in Figure 4 by region 422 to define a p-n junction between the p-type material of the p+ region 420 and the p-well 402, and the n-type material of the additional n+ region 422.

New claim 9 has been added to provide for multiple additional n+ regions (420 and 426 in Figure 4) and at least one additional p+ region (424 in Figure 4).

The amended claim 2 therefore requires at least one p+ and at least two n+ regions in the p-well (one p+ region from the standard structure of an LVTSCR, one n+ region as found in a standard LVTSCR and at least one additional n+ region in accordance with the invention). In contrast, Figure 8 of Ker simply provides the typical LVTSCR structure with first n+ and p+ regions 214, 212 in the n-well and second n+ and p+ regions 220, 222 in the p-well. It also provides for a p+ bulk contact 218. However it does not teach or suggest providing an additional n+ region in the p-well.

The regions of a standard LVTSCR are expressly included in claim 2 insofar as it is relevant to the invention (the n and p-wells, the first n+ and p+ regions in the n-well, and the second n+ and p+ regions in the p-well). The location of the additional n+ region of the invention is also specified as being formed in the p-well. Thus there is no ambiguity about the nature or location of the regions.

35 USC 103

As discussed above, Figure 8 of Ker simply provides the typical LVTSCR structure with first n+ and p+ regions 214, 212 in the n-well and second n+ and p+ regions 220, 222 in the p-well. The

regions 220 and 222 are thus standard regions in an LVTSCR and correspond to the second n+ and second p+ region mentioned in the claim.
Ker does not teach or suggest providing an additional n+ region in the p-well, over and above the second n+ and second p+ regions of the standard LVTSCR.

The examiner states that Ker does not teach in Figure 8B a second n+ and a second p+ region in the p-well but that Ker teaches in Figure 10B the use of external diodes 324 and that Yu teaches a diode formed in a p-substrate. The examiner then argues that it would therefore have been obvious to a person of ordinary skill in the art at the time of the invention to form a diode comprising an n+ region and a p+ region in the p-well in order to reduce the size and simplify the process steps.

The combination of the two references is however inappropriate for the following reasons:

a. The very premise of the present invention is to increase holding voltage in an LVTSCR while avoiding external diodes.
There is nothing in Ker or Yu to suggest combining of the two references. In fact, as discussed above, Ker is seeking to reduce triggering voltage not increase holding voltage. Since Ker is not even dealing with the issue of holding voltage it cannot be said that it would have been obvious to take a reference dealing with triggering voltage and a second reference that happens to provide for a diode in a p-substrate and combine them to provide a solution to a holding voltage problem. The combination of Ker with Yu is therefore simply hindsight reconstruction of the invention based on the teachings of the present application.

b. Further, Yu is a much earlier reference than Ker and if , as the examiner states, it would be obvious to one skilled in the art to combine the references to achieve the benefits enumerated in the present application, why did Ker not do so?

Applicant therefore, respectfully reiterates that Ker lacks explicit elements recited in claim 2. Furthermore, the additional elements of claim 2 are clearly and explicitly claimed. Also it is inappropriate to combine the Ker and Yu references since they deal with a different problem and

there is nothing in either reference to suggest that they should be combined. On the contrary, there is evidence teaching away from the suggestion that it would have been obvious to one skilled in the art to combine the references.

Applicant therefore requests that the finality be withdrawn and the application be allowed.

Respectfully Submitted,

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